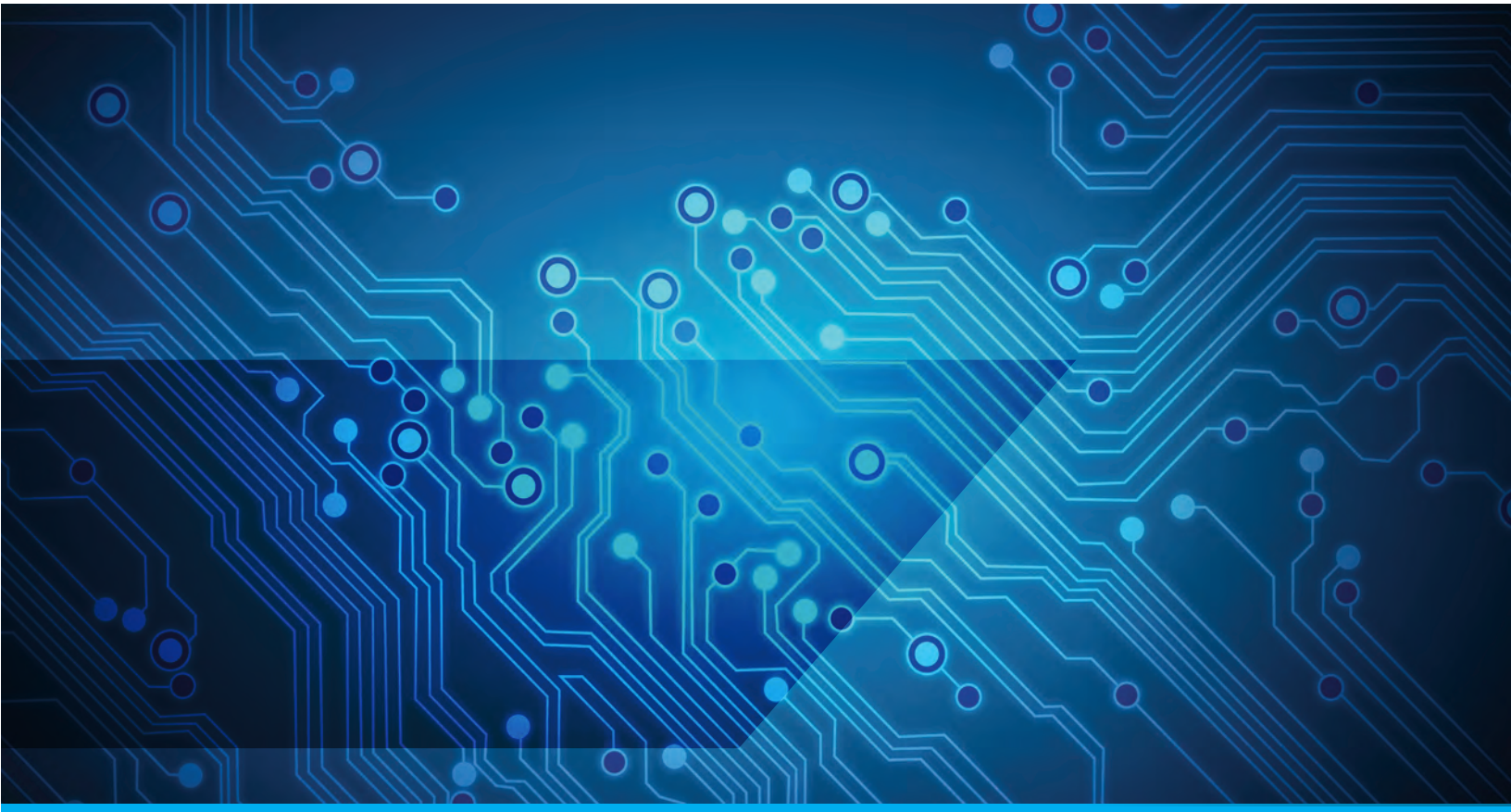
ROW HAMMER IN DRAM

SPIN MEMORY'S FIX AT THE ROOT CAUSE



SPIN MEMORY™

ROW HAMMER IN DRAM – SPIN MEMORY'S FIX AT THE ROOT CAUSE

DYNAMIC RANDOM ACCESS MEMORY (DRAM) IS THE MAIN MEMORY OF ANY COMPUTER SYSTEM.

Invented in the 1960s, DRAM sales now exceed $60 billion per year as the undisputed leader of off-chip working memory. DRAM's architectural simplicity was the reason it was the first commercialized semiconductor memory. Each cell consists of a wordline, a bitline, a capacitor, a bitline contact and a storage node contact as shown in **Figure 1**.

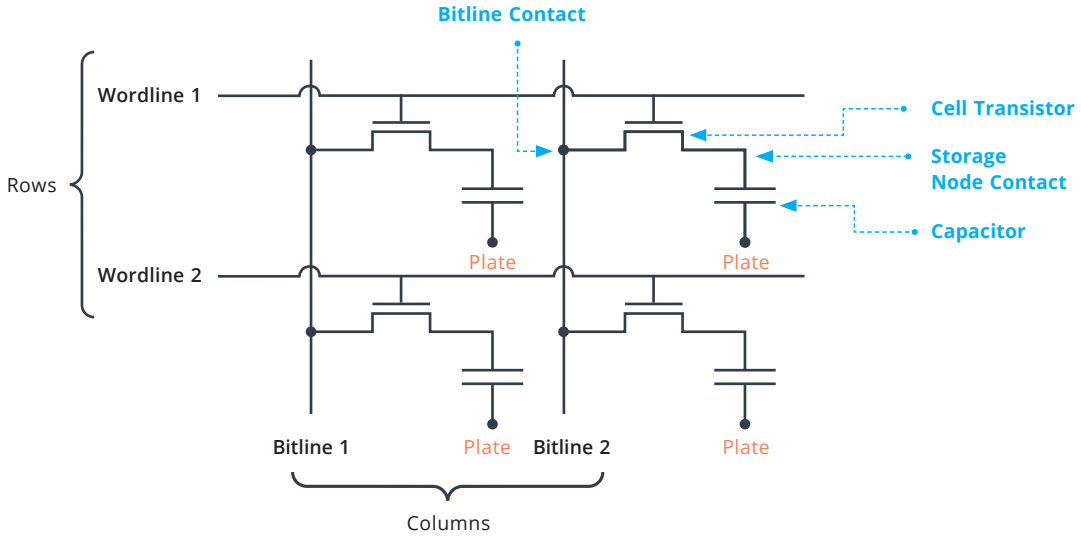


FIGURE 1: FOUR DRAM CELLS IN A MEMORY ARRAY

DRAM retains its vital information in the form of charge stored on each of these tiny capacitors of the memory cell, ranging from 10 to 20 femtoFarads in advanced technology nodes. The charge is transferred to each capacitor using a field effect transistor, but since this transistor plug is not perfect, the circuit leaks and causes the stored charge to decay rapidly, within ~64 milliseconds. This effect has been known since the invention of DRAM in the 1960s and why systems refresh the stored data to restore the capacitor charge with the penalty of significant power dissipation.

All semiconductor memories suffer from what are known as "disturbs" and DRAM is no exception. Simply explained, data in a particular cell can be unintentionally, or worse, intentionally affected by the reading and writing of data in the adjacent cells. Such effects are meticulously measured during the development of each generation of memory technology with containment actions taken in the silicon architecture, chip design and system implementation.

For DRAM, the most important disturb is an effect known as "Row Hammer," first revealed in Kim et al's now famous 2014 paper[1]. Its name comes from the fact that a wordline row can be repeatedly cycled on and

off before a refresh takes place, "hammering" a specific row, causing bit flips in the adjacent rows. The main characteristic of this disturb mechanism is that it grows worse as DRAM scales down. In other words, the effect magnifies as the cells become physically closer. Nefarious actors have been able to exploit Row Hammer to take over complete systems and steal critical data through this technique.[2345]

THE ORIGINS OF ROW HAMMER

Figure 2 shows how Row Hammer operates in a state-of-the-art DRAM array where a cross section of two cells is shown. The transistor channel has a U-shape and the capacitors are connected to storage node junctions situated in the silicon substrate. It would seem that the cells are isolated from each other with deep trench oxide isolation but it turns out there is an exploitable path for the electrons.

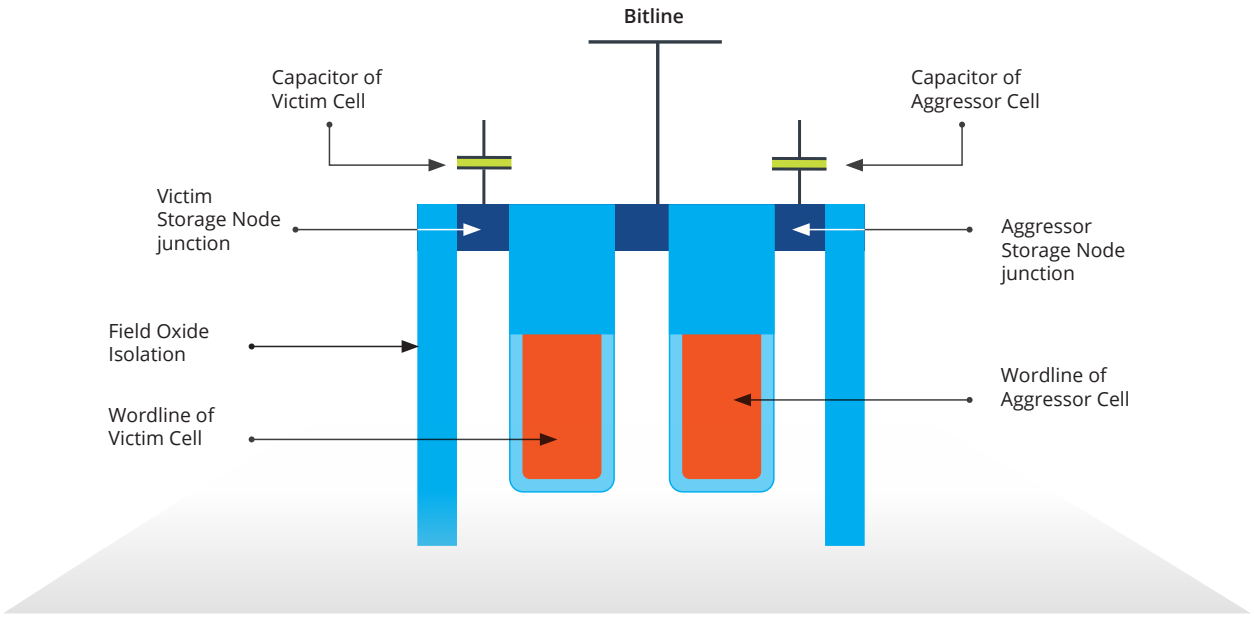


FIGURE 2: CROSS SECTION OF TWO DRAM CELLS IN A MEMORY ARRAY WITH WORDLINE DIRECTION PERPENDICULAR TO PAGE AND BITLINE DIRECTION IN PLANE OF PAGE.

The key to understanding Row Hammer is to follow the migration of electrons in the silicon substrate from the switching "aggressor" cell towards the victim cell. These electrons can have their origins in the aggressor cell's transistor inversion layer which turns off when the aggressor wordline turns off. The electrons can also come from traps which are filled when the aggressor cell's wordline is on.

This is the same charge migration phenomenon that can also cause latch-up, where injected electrons from I/Os can trigger the chip into a destructive low-impedance state. While special guard-rings are placed close to such injectors to "mop up" these electrons before they cause trouble, there is no space between DRAM cells to place such "mops" and DRAM is forced to look for another solution.

Electron migration is necessary but insufficient for Row Hammer to occur. The other essential requirement is that the Storage Node junction is placed within the silicon substrate. This N-type doped junction, metallically connected to the storage capacitor, must be placed in the P-type substrate.

In this arrangement, when positive charge is stored on the victim cell's capacitor, its Storage Node junction is at the same positive potential. Any migrating electrons that reach within a depletion region of this junction will then be collected by the target Storage Node as shown in **Figure 3.** This drops the electric potential of this node and its capacitor. With repetitive hammering of the aggressor cell's wordline, sufficiently large numbers of such electrons can be picked up such that the victim cell's stored data is not readable. In this way, Row Hammering of an aggressor wordline can then flip bits in adjacent victim wordline cells.

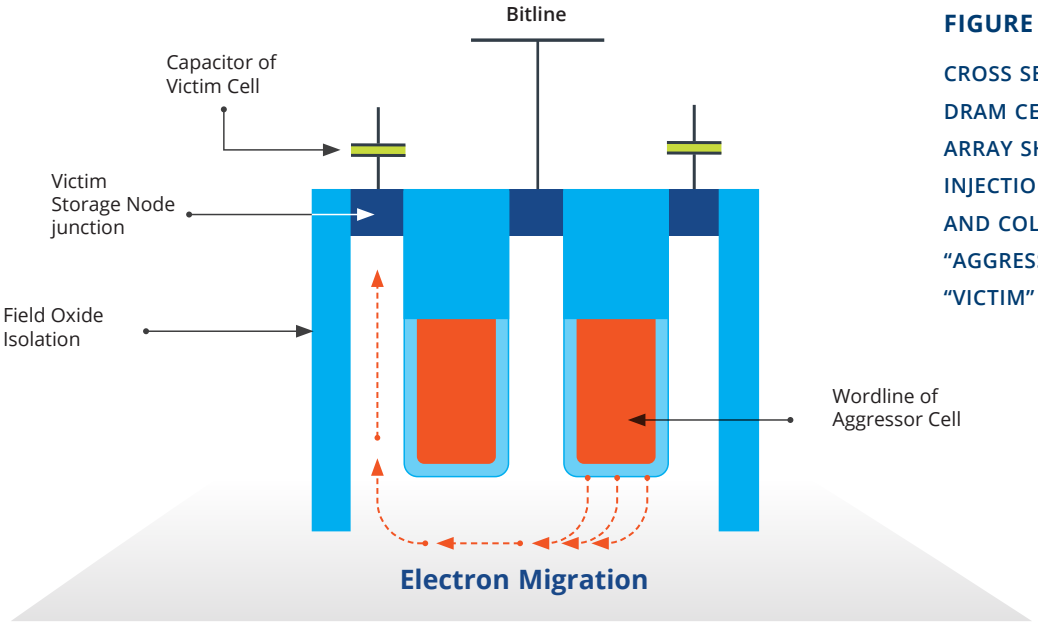


FIGURE 3:

CROSS SECTION OF TWO DRAM CELLS IN A MEMORY ARRAY SHOWING ELECTRON INJECTION, MIGRATION AND COLLECTION FROM AN "AGGRESSOR" CELL TO THE "VICTIM" CELL.

TARGET ROW REFRESH

In 2015, DRAM manufacturers announced a "Silver Bullet" solution: Target Row Refresh (TRR). TRR "fixes" Row Hammer by, in essence, counting the number of times any particular row is accessed and then, after a certain critical number, refreshing all the adjacent cells. This was a celebrated, but unfortunately incomplete, resolution for DRAM manufacturers and their system partners and customers.

In March of this year, a research team, led by the Vrije Universiteit Amsterdam published the result of their research with the unsettling conclusion that "TRR does not solve the Row Hammer problem, and there is no prospect of a solution for this in the near future". In addition, "the new DDR4 chips are even more vulnerable to Row Hammer than their DDR3 predecessors." [6]

Since Row Hammer has been shown to be a way of hacking computer systems, the consequences of this are dire for both DRAM manufacturers and their system customers. Clearly a robust solution is needed to eradicate Row Hammer once and for all. **Spin Memory has the solution to render DRAM immune to Row Hammer.**[7]

SPIN MEMORY HAMMERS ROW HAMMER ONCE AND FOR ALL

Spin Memory has developed a solution for Row Hammer that fixes it at its root cause by immediately sweeping away any electrons injected from the aggressor cell before they reach any victim cell's Storage Node junction. Spin has developed a new vertical, selective epitaxial cell transistor whose channel has a low enough doping concentration that it operates in full depletion.

The fully depleted channel cell transistor leads to a crucial architectural change allowing the transistor channel body to be completely electrically isolated from the silicon substrate. This leads to complete electrical isolation of the DRAM cell's Storage Node from the substrate and eliminates the possibility of migrating electrons reaching any Storage Node junction.

The DRAM manufacturers are exploring vertical cell transistors through silicon pillar etching and implantation. This results in partially depleted channels that force them to connect the transistor channel body directly to the substrate. This approach results in the Storage Node junction remaining in the silicon substrate and therefore still prone to Row Hammer. **Figure 4** shows a cross section of two DRAM cells implemented with Spin Memory's approach.

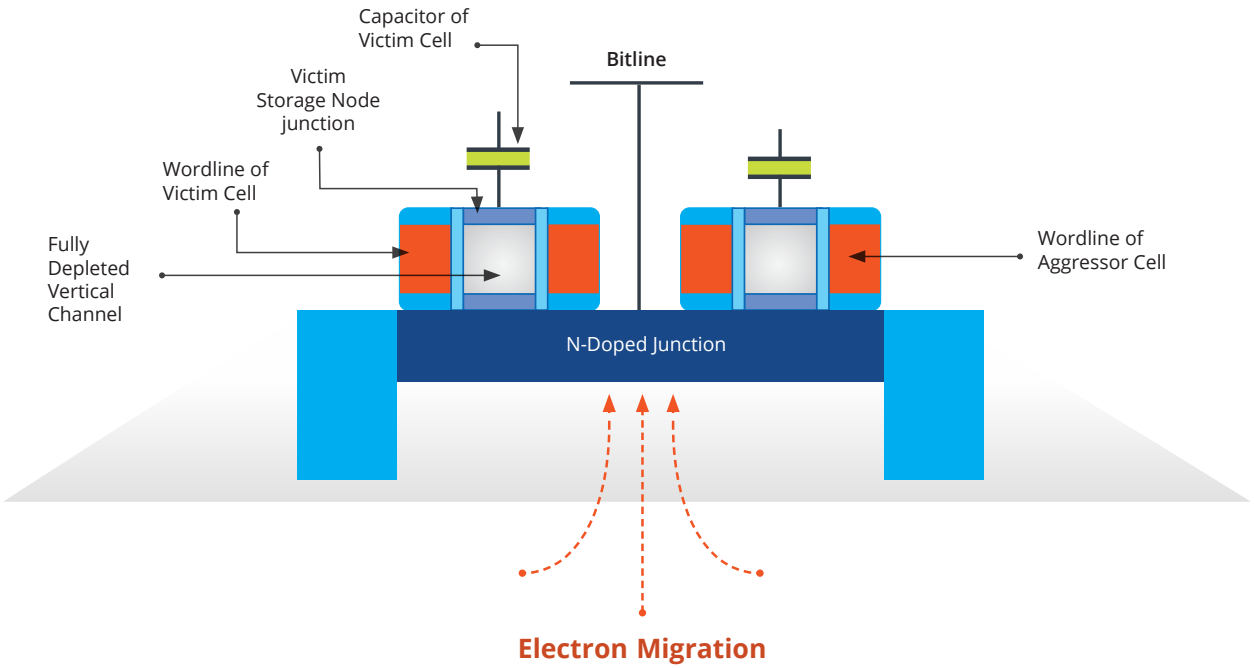


FIGURE 4: CROSS SECTION OF TWO DRAM CELLS IN A MEMORY ARRAY USING SPIN MEMORY'S FULLY DEPLETED VERTICAL CHANNEL CELL TRANSISTORS. FULL DEPLETION ALLOWS THE CHANNEL TO BE ISOLATED FROM THE SUBSTRATE AND THEREFORE ISOLATES THE STORAGE NODE JUNCTIONS TOO.

Spin's vertical cell transistors with full depletion allow the channel body to be isolated from the substrate. This in turn isolates all Storage Nodes from the substrate by default as shown in **Figure 4**. Migrating electrons in the substrate can no longer be collected by the Storage Nodes. This approach has the significant benefit of being a smaller total cell area when compared to today's DRAM.

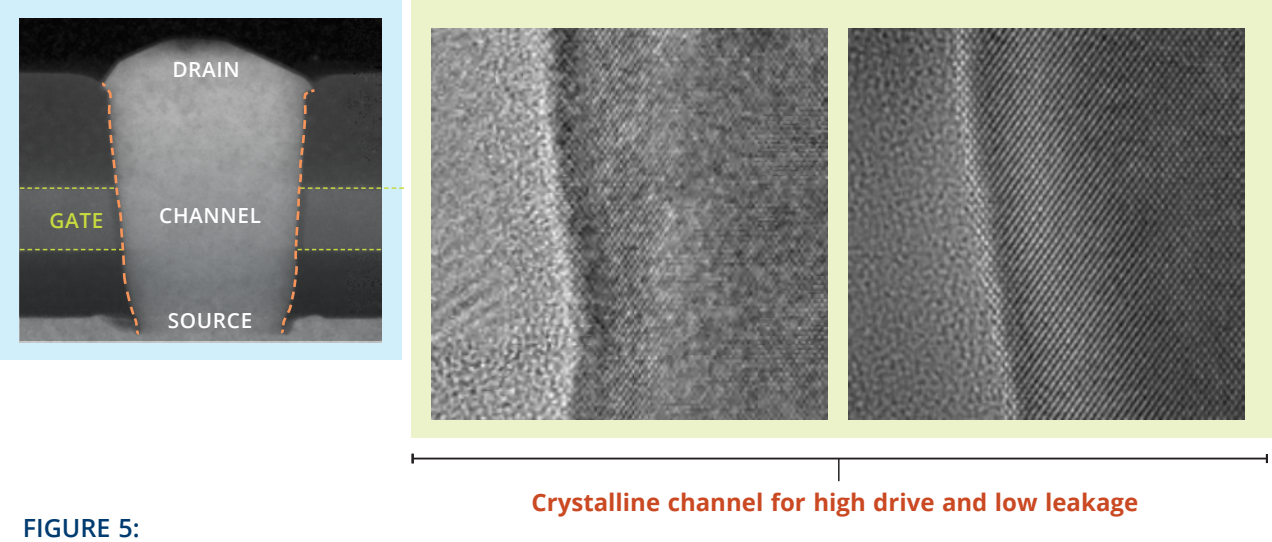


FIGURE 5:

ELECTRON MICROGRAPHS OF CROSS SECTIONS OF THE SPIN MEMORY FULLY DEPLETED CHANNEL VERTICAL TRANSISTOR.

Figure 6 shows a Technology Computer Aided Design (T-CAD) Row Hammer simulation comparing classic DRAM with Spin's DRAM approach. The victim cell's Storage Node electrical potential is plotted as a function of the aggressor cell's number of on-off activations. The classic DRAM electrical potential reduction with aggressor cell activations is the hallmark of Row Hammer. If enough activations are done to make the victim cell's data unreadable before a refresh can take place, then the Row Hammer hacker has done his job to corrupt precious data. The immunity to Row Hammer of Spin's solution is clear.

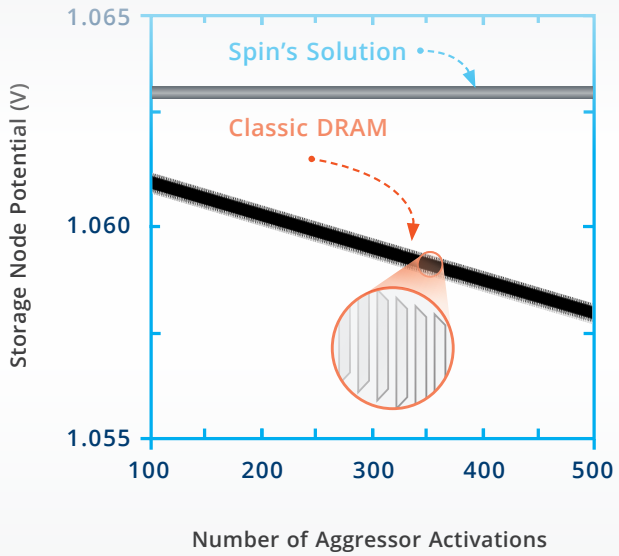


FIGURE 6:

T-CAD SIMULATIONS OF ROW HAMMER IN CLASSIC STATE-OF-THE-ART DRAM VERSUS SPIN MEMORY'S SOLUTION. THE STORAGE NODE POTENTIAL OF THE VICTIM CELL IN CLASSIC DRAM DROOPS AS A FUNCTION OF THE NUMBER OF ON-OFF AGGRESSOR CELL ACTIVATIONS. SPIN'S SOLUTION IS IMMUNE TO ROW HAMMER.

CONCLUSION

Spin Memory has developed a fully depleted vertical channel transistor that solves Row Hammer once and for all. It also allows for a more compact memory cell reducing the overall cost of DRAM. These developments have potentially far-reaching consequences.

REFERENCES & FOOTNOTES

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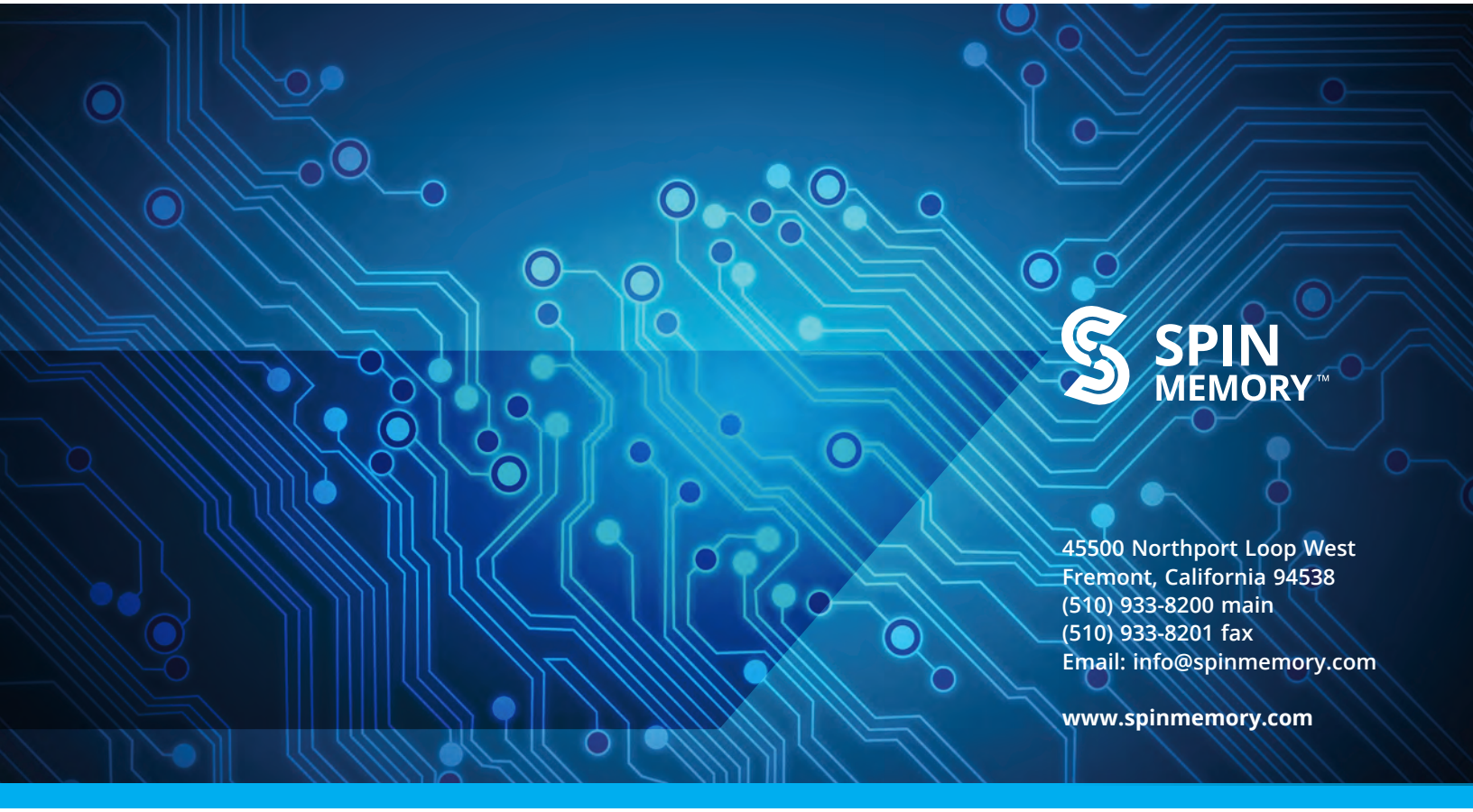

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